

# Pin electronics test and debug using PXI test station

By Brian Foley

Fairchild is one of the largest independent semiconductor companies focused solely on multi-market products. Fairchild designs, develops, and markets analog, mixed signal, discrete, logic, interface, optoelectronic, and non-volatile memory semiconductors. To test these products, Fairchild utilizes many test systems with different architectures and topologies.

One of these testers, a 1980's vintage logic test system required upgrading due to maintenance and obsolescence issues. The system had 64-Pin Electronics Cards (PEC), each with one Parametric Measurement Unit (PMU) and one functional channel for a total of 64 tester channels. A new PEC, designed by Fairchild with the assistance of students and staff of the University of New Hampshire, needed a tester for debug, verification, and repair. The new PEC uses current industry standard ATE components to replace the older discrete designs.

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The new PEC design, shown in Figure 1, has four mini (low current  $\pm 40\text{mA}$ ) PMUs and one  $\pm 500\text{mA}$  main PMU. The system wide reference levels for VIL, VIH, VOL, VOH, and threshold voltage have been replaced with per pin

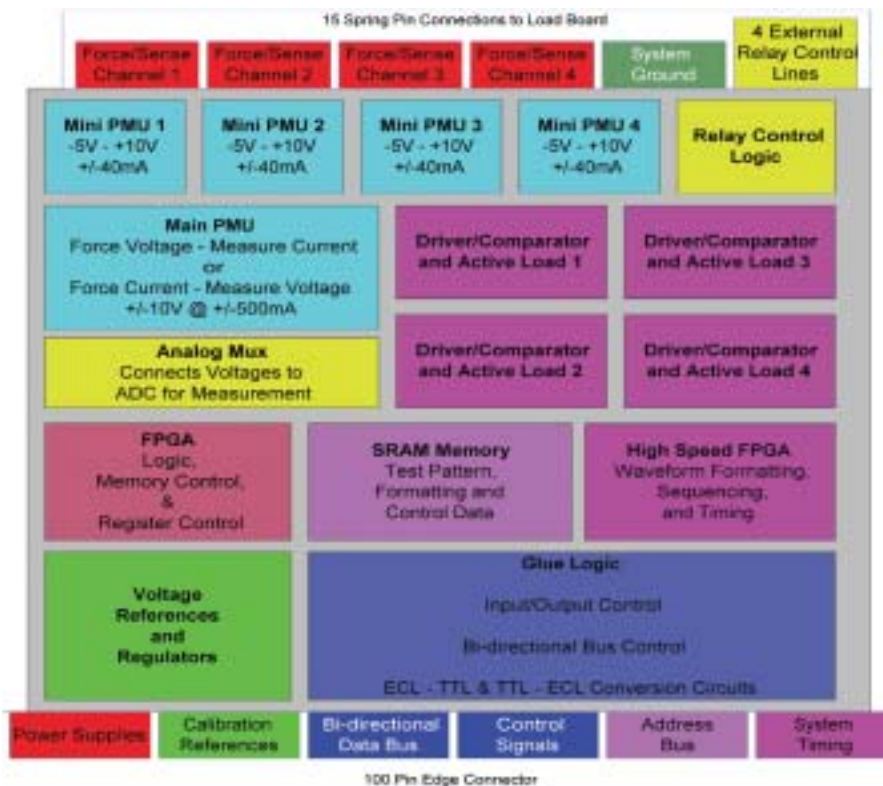


Figure 1

DACs for these functions, enabling per pin input and output functional levels. The number of functional test channels has also increased from one to four per PEC. This increases the total test channels from 64 to 256. This allows Fairchild to test up to four times more devices in parallel than the older system with better resolution and accuracy without any additional floor space requirements. The only other option would have been to purchase a new ATE tester at a much higher cost per system.

## The test requirements

The new PEC cards require both analog and digital stimuli/response to perform an effective functional test. The PEC test set required the following signals.

There are 64 Digital I/O Lines. The application requires up to 15 MHz Data and Clock Rate at TTL levels (Geotest GX5150 and GX5151 DIO, 6U PXI 50 MHz Data Rate). The Digital I/O is used to control and setup all functions and measurements of the PEC under test. All of the register loading, memory data and control, DAC and ADC control, and read back are performed using these two cards. They have a very flexible command set that allows all functions of the DIO to be reconfigured without having to load a new pattern file. This application uses some of these features:

- A blank pattern is written to memory on the first pattern load.
- The address, page, and data are written to each corresponding memory location.

The memory pointer is set to the start address of the same pattern and run, eliminating the need for additional patterns or pattern loads. Each DIO card can be used in either a read or write mode – this can be changed only when no patterns are executing. This method is used to read and write data to the bi-directional bus. A different memory location is used to load the read and write patterns, the card mode is changed, and the memory pointer set to the corresponding address.

The following is a listing of the digital control signals that are used in this application (Digital I/O requirements for PEC debug and repair station):

- 18 Digital Control Lines
- 7 Digital Input Lines
- 16-Bit Bi-directional Bus
- 12-Bit Address Bus
- 4 Lines ECL to TTL and 3 Lines TTL to ECL Conversion (performed with logic conversion ICs)

### Selected test equipment

**128-Channel Scanner/Multiplexer:** Used to connect internal references, external power supplies, temperature sensors, and flying probe prober to the test system (GeoTest GX6264, 6U PXI). This multiplexer can be connected in several configurations, including 128 single-ended or 64 differential channels.

**24 Relay Control Channels:** Used to control resistive loads for force current; measure voltage, force voltage, current verification; power supply control and verification (National Instruments 6527 Optically Isolated Digital I/O, 3U PXI). Using an optically isolated relay controller allows relays of different voltage levels and signals of different levels to be used in the same application. This also allows the use of external supplies to be used, removing the additional load on the chassis supplies, and eliminating the switching current of the relays from affecting the overall noise level of the system.

**6 1/2 Digit Digital Multimeter:** Used for accurate voltage, current, resistance, capacitance, impedance, frequency, and leakage measurement (Geotest SMX2044 6-Digit DMM/LCR, 3U PXI). The SMX2044 is not just a standard DMM. It also has functions most often seen only on LCR meters. It also has a force voltage – measure current function is useful for leakage measurements.

Other functions include pulse width, totalizer, temperature, 6 wire ohms, AC and DC voltage source, as well as DC current source.

**16 Voltage References (DACs), 16-Bit resolution each:** Used as external voltage references and calibration references (Alphi DAC 16, CompactPCI). This card was added to the test system to allow debug and verification of the older design PEC, which requires external references for input and output volt-

age, current, and threshold levels. These DACs can also be used as reference and control voltages as needed.

**Chassis/mainframe:** A PXI Chassis with an embedded controller is used to accommodate the selected PXI cards (Geotest GX7000 6U PXI Chassis – see Figure 2). The PXI chassis provides an internal hard drive, floppy, CD-ROM, and uses several PCI bridges to extend the PCI Bus up to 20 slots. Slot 1 is dedicated for either an embedded controller or a PCI to PXI remote controller card. In this application, an embedded controller is used to reduce system space (Geotest GX7900, 6U PXI). This controller has a Pentium CPU, VGA, Ethernet, serial, parallel, and USB ports.

Flying probe prober with 1 mil (.001 inch) accuracy and camera for probe to PCB alignment: This prober was selected to enable testing of the very fine pitch surface mount components. A standard meter or oscilloscope probe is several times larger than the space between pads. This can result in shorted leads and device failure. The prober (Huntron ProTrack Prober II) also enables increased throughput using automation. This prober is both accurate and a small enough platform to be used as part of a bench-top test system. The prober is connected to both the DMM and Digital I/O through the scanner allowing the probe to be used to measure all functional, DC, and analog functions on the PCB under test.

### External test hardware

The test instrumentation is connected to the PCB under test using two circuit boards that connect the 100-pin edge connector at one end and the spring probes on the other. The PCB on the edge connector side has all of the power supply control and measurement relays as well as the ECL–TTL and TTL–ECL translators. All signals have a protection circuit that consists of the series resistor and voltage clamp (Zener diode). This prevents a defective board from back driving signals or exceeding the maximum rated voltage for any of the I/O. This PCB also contains the two precision voltage references that are used to calibrate the main ADC of the board under test. The latches used for the low speed inputs on the board under test are also contained on this PCB.

The second PCB that is connected to the spring pins (load board connections) consists of several relays and precision resistors that are used to verify and calibrate both the mini and main PMUs. The DMM is used to verify accuracy and calibrate all voltage and current forces and measurements. The functional driver and loads are also verified and calibrated using this PCB. All functional input and output data from the functional drivers are cabled back to the Digital I/O cards for input and output data verification. The last function that is performed on this PCB is the load resistors that are used to simulate the maximum coil resistance of relays controlled by the open collector relay drivers. The scanner channels are used measure across each of these resistors in order to verify proper operation.

### Why PXI was chosen over VXI or GPIB

To determine which platform would be most suitable for this application, Fairchild evaluated GPIB, VXI, and PXI with the following considerations:

- GPIB, while still a viable interface for certain applications, proved inadequate for this application due to data frequency, triggering, and integration requirements.
- Both VXI and PXI met the application requirements; therefore the selection came down to cost. A VXI system would have cost at least \$20,000 more than its PXI equivalent. Since that amount was nearly 100 percent more, the selection was easy.

### The test program

The test program for this application combines several different types of equipment and interfaces. This includes the PXI and CompactPCI instruments, the prober, camera, and networking. All PCBs are tracked by serial number and date tested. This generates a running history of all boards that are tested and a database that is used to debug all future PCBs. This data is used to in an automated failure lookup table that will grow as more failures are debugged. Initially most cards will require a semi-automatic debug process of all test nodes to evaluate their normal signature.

The camera in the Huntron Prober is used to align the PCB to the flying probe. This is done using a two-point alignment, two targets are selected on the PCB and stored. The same two targets are then aligned on the board under test and global X and Y offsets are generated. These offsets are used to correct for any variation in the PCB placement in the test fixture and variation from board to board.



**Figure 2**

All CompactPCI, PXI, and prober DLLs were used as received from the vendor. The DLL is simply added to the compiler along with the required files and that device is ready for use.

An untested PEC is first checked for shorts across all the power supplies to each other and ground. This is performed to prevent powering up a PCB with direct supply shorts that can damage the board itself and possibly the test station. If all supply connections pass verification, the board is powered up and the programmable gate arrays are programmed from an on-board EEPROM. The next step is a quick verification of all the subsystems to verify that they are all operational and accessible. Any subsystem failure will flag additional verification of that circuitry, when the quick verification is complete. The Huntron Prober test probe is then run through the circuitry comparing each node to its normal electrical signature. This could include any of the following: VAC, VDC, frequency, pulse width, duty cycle, capacitance, inductance, and functional pattern verification. The failure signature is then compared to failures of previous boards tested and a repair recommendation generated. This could include inspecting and reworking the board for possible solder shorts at a particular node, replacement of a failing part, or manual verification if the failure mode had not been encountered before.

This is when the Sun-up PCB Viewstation is very helpful. The software can be used to show all connections to a fail-

ing node. These connections many times are on both sides of the PCB and can span the entire PCB. Manually tracking down these nodes using schematics is time consuming as the technician must keep referring to the schematic and assembly drawings in order to track down all connections to a failing node. This information is then added to the database so that any future failures of the same type are flagged for the same repair. See Figure 3 for a sample Viewstation screen.



**Figure 3. Sun-up Viewstation display**

Figure 4 is a copy of the user GUI graphical interface used by this application. It includes the camera image and PCB layout drawing for the component under test. The operator is also able to run the station in semiautomatic mode by placing the camera cross hairs over the point he wishes to probe and by pressing the Move to Node button. This allows the operator to contact any location on the PCB to within  $\pm$  mil (0.001 inch) without the risk of shorting component leads or probing the wrong location.

Software packages used in this test application include the following:

- National Instruments LabWindows/CVI. Used to write all C-based test and control code for the test system, as well as the GUI interface used to control and display all of the data including the camera image and PCB component and pad location.
- Sun-Up PCB Viewstation. Used to view PCB layout files after conver-

sion of Pads files. Indicates PCB device and pin locations, as well as all connections to a given node. The Viewstation is useful in PCB debug as all connected nodes can be viewed at once. This tool is also used to generate the X and Y coordinate list from the PCB layout file that is used by the prober.

- Huntron PCB Converter. Converts PCB pads data file to X, Y, and Z coordinate files for Huntron Prober.

- Huntron Control Software. Used to control both the prober and camera using a serial port for the prober and a custom interface for the camera.

### Conclusion

This project has been the first use of a PXI or CompactPCI test system by our engineering department and likely not the last. The integration and operation of equipment from several different vendors was seamless, all equipment operational, and performed as specified. Fairchild will definitely consider PXI and CompactPCI instrumentation for future test requirements.



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and tester interface hardware design, as well as ATE and PC based IC and module test programming. Brian graduated from New Hampshire Technical Institute in 1980 with an Associate in Electrical Engineering.

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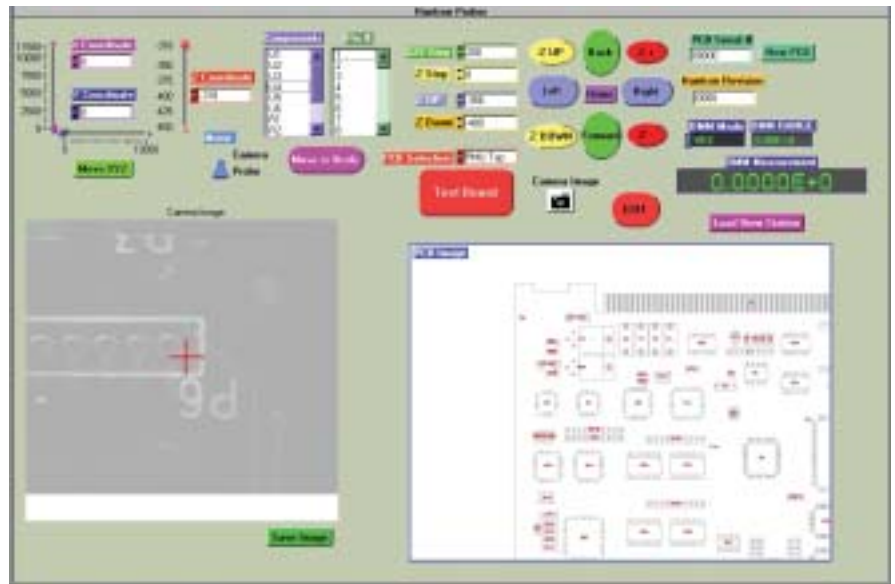


Figure 4. Test set's user interface